Templado System

RISC-V Payment Gateway:
A Secure and Efficient Solution

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Abstract

This white paper presents the design and implementation of a payment gateway using the RISC-V instruction set architecture (ISA). RISC-V is an open-source, extensible ISA that offers numerous advantages in terms of flexibility, scalability, and security. By leveraging the unique features of RISC-V, we propose a robust payment gateway solution that enhances transaction security, accelerates processing speed, and ensures compatibility with existing payment systems. This paper outlines the key components, benefits, and implementation considerations of the RISC-V payment gateway, highlighting its potential to revolutionize the payment processing industry.

Introduction

In the fast-paced digital era, the need for secure, efficient, and scalable payment gateways has become paramount. As the backbone of modern financial transactions, payment gateways must ensure seamless and reliable communication between customers, merchants, and financial institutions. To meet these ever-increasing demands, technological advancements are essential. One such innovation is the utilization of RISC-V processors, which have emerged as a game-changer in the field of computing.

RISC-V, an open-source instruction set architecture (ISA), has gained significant traction in recent years due to its flexibility, extensibility, and potential for customization. Unlike proprietary processor architectures, RISC-V offers a level playing field for both established players and emerging startups, fostering innovation and collaboration in the industry. Its open nature enables developers to create highly efficient and tailored processors that can cater to specific use cases, including payment gateways.

This white paper aims to explore the transformative potential of RISC-V processors in the realm of payment gateways. By leveraging the unique advantages of RISC-V, payment gateway providers can enhance security, improve performance, and reduce costs, thereby revolutionizing the way financial transactions are processed.

The European Union will release €270 million in funds as it tries to attain technology independence by building chips based on the open RISC-V instruction set architecture.
The EuroHPC Joint Undertaking (EuroHPC JU) has published an upcoming call for proposals to fund a project targeted at building high-performance computers based on RISC-V hardware and software.

This is a big commitment by the European Union to create a computing infrastructure based on

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RISC-V, which is an open instruction set architecture. RISC-V is free to license and has just a handful of instructions in the base architecture. Chip designs can tack on custom modules and accelerators.

Europe is building a native RISC-V chip to cut reliance on proprietary x86 and Arm architectures. The European Commission has also passed the European Chips Act to boost its computing infrastructure, and has referenced RISC-V multiple times in the legislation.

At the October 2022 conference, Alibaba also announced its open-source RISC-V-based Xuantie series processors and related tools and system software. Another milestone in the RISC-V ecosystem after its release of Xuantie 910 and other processors. It is said to be one of the first such commercial processors globally, further pushing RISC-V architecture's maturity and integrating software with hardware development.

Thanks to its flexibility, simplicity, and being of open source, the RISC-V architecture has become an increasingly popular choice in IC design. By harnessing the power of RISC-V processors, payment gateway providers can unlock a new era of efficiency, security, and scalability. The possibilities are vast, ranging from streamlined transaction processing to enhanced fraud detection and prevention. This white paper will serve as a comprehensive guide for stakeholders in the payment gateway industry who are interested in leveraging RISC-V to drive their businesses forward.

RISC-V architecture

In the ever-evolving landscape of computer architecture, the RISC-V (Reduced Instruction Set Computer - Five) instruction set architecture (ISA) has emerged as a groundbreaking and disruptive force. Developed at the University of California, Berkeley in 2010, RISC-V has gained substantial traction and garnered widespread attention due to its open-source nature, scalability, and extensibility.

Whether it be a microprocessor, a microcomputer, or a regular desktop computer, their processors all use an instruction set architecture (ISA). An ISA is the part of the processor that contains all the basic instructions a processor can execute. These instructions are the building blocks of a computer program. They are usually not more complex than your basic addition and subtraction. In general, there are two types of ISA circulating in the market. They are the RISC and CISC architectures. RISC stands for Reduced Instruction Set Computer, while CISC stands for Complex Instruction Set Computer. Both architectures are prevalent today, with x86 (Intel and AMD processors) being the top processor utilizing CISC and ARM as the most popular RISC architecture.

RISC-V is an open-standard ISA developed at the University of California, Berkeley. This ISA doesn't introduce any new technology in the market, yet many speculate it is the future of RISC-based processors.

The great thing about RISC-V is its ability to expand the instruction set based on whatever processes your chip will need for a given product. RISC-V only starts with a base instruction set of 47 instructions. These instructions include all the basic functionalities a chip needs to work and do basic tasks.
Designers will then be free to choose which instructions to add to the base instruction set to give the chip all the functionalities it needs without any extra bloat functionalities it wouldn't use.
Although RISC-V is still a relatively new ISA, its potential to provide cost-effective and highly efficient specialized chips for various applications is what makes it a special ISA.

RISC-V has gained attention from companies like Amazon, Google, Qualcomm, Intel, Rockchip, SiFive, Sony, ZTE, and Western Digital. This is because RISC-V is an open-standard ISA. RISC-V International (a non-profit association for RISC-V) allows anyone to use the RISC-V ISA on their processors without paying a fee.

RISC-V license-free

There are several advantages to RISC-V being license-free. Here are some key benefits:

- Open and Transparent Ecosystem: RISC-V's license-free nature promotes an open and transparent ecosystem. It allows anyone to access, study, modify, and contribute to the design and implementation of RISC-V processors and related technologies. This openness encourages collaboration, innovation, and community-driven development.

- No Royalties or Licensing Costs: By eliminating the need for licenses and royalties, RISC-V provides cost advantages to organizations and individuals. Users can freely implement RISC-V processors in their products without incurring additional expenses, enabling greater accessibility to the architecture across a wide range of applications, from small embedded devices to large-scale computing systems.

- Vendor Independence: The absence of licensing restrictions fosters vendor independence. Companies can design, develop, and manufacture RISC-V-based products without being tied to a specific vendor or facing vendor lock-in. This freedom allows businesses to choose the best options for their needs, such as customizing processors to optimize performance, power consumption, or security.

- Accelerated Innovation: RISC-V's license-free nature spurs innovation and rapid development. It encourages a diverse community of researchers, academics, and industry professionals to collaborate, share ideas, and create new technologies. This leads to faster advancements in processor architectures, specialized accelerators, software tools, and other related domains, benefiting the entire ecosystem.

- Customizability and Specialization: The license-free nature of RISC-V enables customization and specialization at various levels. Users can modify and extend the RISC-V instruction set architecture (ISA) to meet specific requirements, tailoring it to their unique applications and optimizing performance. This flexibility is particularly valuable in domains such as Internet of Things (IoT), machine learning, and embedded systems, where tailored solutions often yield significant benefits.

- Security and Trust: With RISC-V being license-free, security and trust can be enhanced. The open nature of the architecture allows thorough scrutiny by a broad community of experts, leading to the discovery and mitigation of vulnerabilities or design flaws. The transparency and ability to audit the design and implementation can help build trust in the processor's security features, making it suitable for sensitive applications.

- Education and Research: RISC-V's license-free status benefits educational institutions and research organizations. Students, researchers, and academics can access and experiment with RISC-V architectures without any restrictions, facilitating learning, experimentation, and exploration of computer architecture concepts. This accessibility encourages academic collaboration, promotes knowledge sharing, and helps drive forward the field of computer science.

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RISC-V economic sanction free

- One advantage of RISC-V being economic sanction-free is that it promotes international collaboration and avoids potential restrictions on the use of the architecture due to economic sanctions imposed by certain countries. Here are some key points related to this aspect:

- Global Accessibility: RISC-V being economic sanction-free ensures that developers, researchers, and businesses from all around the world can freely access and utilize the architecture without being impeded by economic or trade restrictions. This enables a diverse and inclusive community to contribute to the advancement of RISC-V and fosters global innovation.

- International Collaboration: The absence of economic sanctions allows for international collaboration on RISC-V projects. Developers and organizations from different countries can freely collaborate, share knowledge, and collectively work towards improving the architecture and its ecosystem. This collaborative environment encourages the exchange of ideas and diverse perspectives, leading to more robust and innovative solutions.

- Mitigating Geopolitical Risks: Economic sanctions imposed on specific countries can create uncertainty and introduce geopolitical risks for technology development and adoption. By being economic sanction-free, RISC-V offers a neutral and reliable option for organizations seeking to avoid potential disruptions or limitations resulting from geopolitical tensions. It provides a stable foundation for building and deploying technology solutions across borders.

- Market Expansion: The economic sanction-free nature of RISC-V helps facilitate its global market expansion. Companies can confidently invest in RISC-V-based products and technologies, knowing that they won't face restrictions or complications related to economic sanctions. This opens up new opportunities for businesses to explore international markets and reach a broader customer base.

- Technology Independence: RISC-V being economic sanction-free contributes to technology independence. It allows organizations to reduce their reliance on architectures or technologies that may be subject to economic sanctions. This independence empowers businesses to have more control over their technology roadmap, ensuring continuity and avoiding potential disruptions in the face of changing geopolitical dynamics.

Who cares about RISC-V

China cares. As a result of recent US sanctions, Chinese manufacturers have lost or fear losing access to x86 or Arm ISAs. Even if trade policies change, Chinese companies would remain aware that, at any future point, the “ISA rug” could get pulled out from under them. Going the RISC-V route could give them a way around that possibility, helping China meet its aggressive goals for reducing reliance on chip imports. The country has been trying to become more self-sufficient in making chips for years, although this has seen some challenges. About a third of RISC-V organization members are from China, and multiple large Chinese companies have announced RISC-V chips already.

Startups care. In the three years between 2020 and 2022, venture capitalists (VCs) will invest about US$22 billion into startup chip companies of all kinds. To put this into perspective, that’s more than

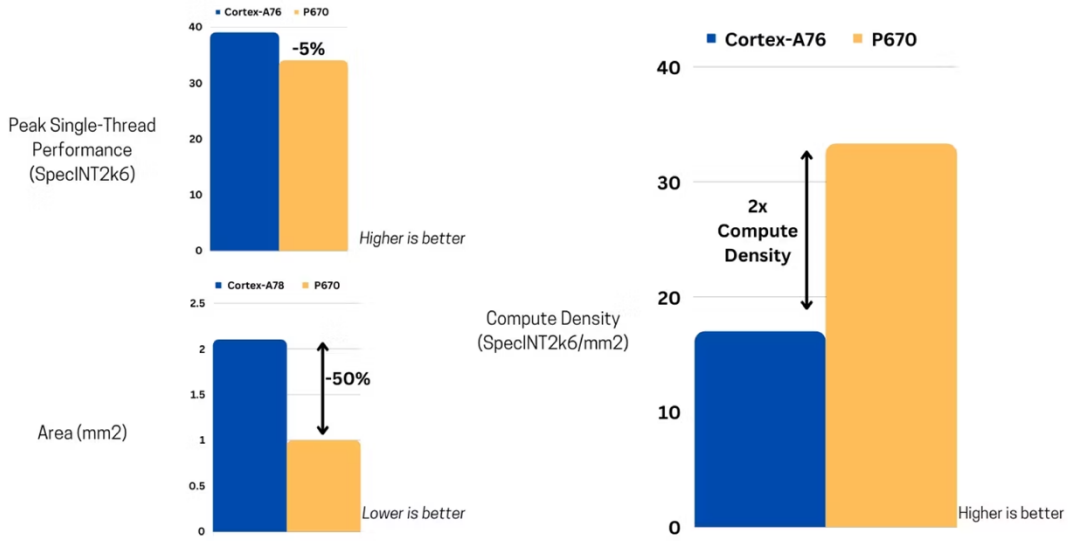
the US$21 billion they invested in the entire 11 years between 2005 and 2016. All that money means more chips being made—but startups usually must make them on a budget. A million-dollar license fee may not matter to one of the world's largest smartphone companies, but it does matter for a startup that has relatively little cash and a monthly burn rate. It's not surprising that, according to a 2020 study, more than 23% of new ASIC (application-specific integrated circuit) and FPGA (field-programmable gate array) chips from startups incorporated at least one RISC-V processor.

AI cares. A number of new AI chip designs appear to be using RISC-V. Interestingly, expectations were that the technology would not be used in data centers in the near term, but some speculate that AI chips may allow RISC-V to break into the data center market earlier than expected.

Foundries care a bit. Although ISAs don't matter much to those who actually make the chips, it is possible that RISC-V, with its lower cost and greater flexibility, could lead to a Cambrian-style explosion in new chip designs. Hundreds or thousands of new chips may need to be manufactured by foundries, in low volumes at first, but any potential boom in new chip designs would be a tailwind for semiconductor manufacturers.

ARM or RISC-V? Which is Better?

ARM and RISC-V are ISAs that follow the RISC design philosophy, so which one is better?
To compare, here is the performance comparison between SiFive's P670 processor vs. Arm's Cortex-A78 processor:



As you can see in the illustration, the Cortex-A78 is slightly ahead of the P670 regarding peak single-thread performance. Although the Cortex-A78 wins in raw performance, the P670 doubles the compute density of the Cortex-A78. This means that SiFive's P670 processor provides comparable peak single-thread performance over the Cortex-A78, which is twice the physical size of the P670.

In this comparison, SiFive's P670 processor wins over Arm's Cortex-A78 for delivering comparable single-thread performance at half the size. However, you should also note that the Cortex-A78 was

released on December 2020 through the Vivo X60 and X60 Pro, while the P670 was just announced on the first of November 2022.

RISC, RISC-V, and ARM are Different Instruction Set Architectures

In summary, RISC is a design philosophy that uses fewer instructions than you would find on a regular desktop processor like the x86. Having shorter and fewer instructions allows RISC processors to be highly power efficient.

ARM is a closed-source ISA based on RISC that is licensed to companies for their processors and SoCs. The ARM ISA allows Arm to design high-performance RISC processors like Apple's M1 chips. On the other hand, RISC-V is an open-standard ISA based on RISC that anyone can use to design

their own chips without paying license fees. Its open-source nature allows the RISC-V ISA to be further modified and expanded to make specialized chips for specific tasks.

Although it might not seem to be all that important, this ongoing competition between ARM and RISC-V will surely benefit all consumers, especially when it comes to IoT devices, microcontrollers, single-board computers, and handheld devices such as smartphones and tablets. And who knows, with Apple's M1 chips as proof, RISC-based processors may actually compete with x86 processors sooner than expected.

RISC-V for Servers

The ability to spin up custom chip designs at a lower cost has made the RISC-V architecture attractive for devices that don't require cutting edge chips.
Ventana Micro Systems is now bringing that ability to RISC-V chips for servers, with plans to release chips for high-performance computers in the future. Ventana said it plans to cut the time and cost required to design server chips, which typically have multi-year design, validation and testing cycles. The company announced its Veyron V1 chip, which the company said provides comparable performance to chips based on x86 and Arm architecture. Chips from Intel and AMD are based on the x86 architecture, and major cloud providers are providing cloud instances running on Arm-based chips from Ampere Computing.
With Veyron, companies will not have to wait three to four years to get a final chip.

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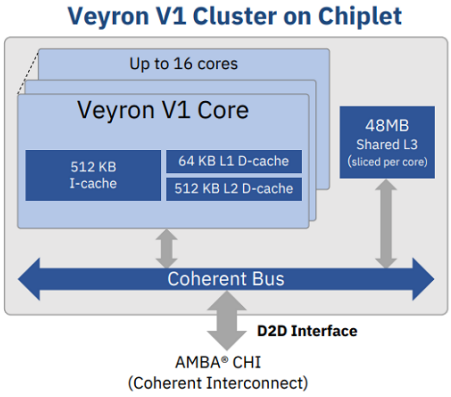
Ventana Veyron V1: Highest Performance RISC-V CPU



- Eight wide, aggressive out-of-order instruction pipeline
- 3.6GHz
- 5nm process technology
- 16 cores per cluster
- High core count multi-cluster scalability (up to 192 cores)
- 48MB of shared L3 cache
- Advanced side channel attack mitigations
- IOMMU & Advanced Interrupt Architecture (AIA)
- Comprehensive RAS features
- Top-down software performance tuning methodology
- Customer samples mid ‘23

Some European researchers are developing open-source RISC-V cores to compete with x86 and Arm, and are relying on only €8 million in funding.
Details about the ambitious eProcessor project were shared at the International Supercomputing Conference (ISC) in Hamburg, Germany. The conference is a showcase for pan-European high-performance computing projects.
The project’s goal is to develop building blocks – including single-core and multi-core RISC-V cores – for European organizations building basic computing devices or high-performance systems. The researchers are developing other modules, such as AI cores, that can be tacked on to RISC-V CPUs. The researchers are topping off the chip designs with a complete open-source software stack, including the OS. System builders will get a full stack of offerings to build RISC-V systems while keeping the cost minimal.
Many researchers are building RISC-V cores, but the eProcessor is ambitious in scope. It is operating on funding of €8 million, with €4 million from the EU. It is similar to work being done by fabless chip designers developing both the hardware and software.

LeapFive launches NB2 RISC-V flagship SoC in China.
The showcased NB2 SoC features four RISC-V cores. The NB2 SoC includes four RISC-V cores produced by SiFive, as well as an iGPU, NPU and VPU. LeapFive employed 12 nm nodes to produce the chips and also offers motherboards that expand the SoC capabilities with additional ports and features.

The Chinese Academy of Sciences has unveiled a new high-performance processor chip and a new operating system, based on the popular open-source chip design standard known as RISC-V.
The chip has been named Xiangshan open-source high performance RISC-V processor, while the operating system is called Aolai. These technological achievements represent China's commitment to building an open-source chip ecosystem with a new blueprint to support its digital economy and promote international cooperation in chip development, experts and officials said on Friday.

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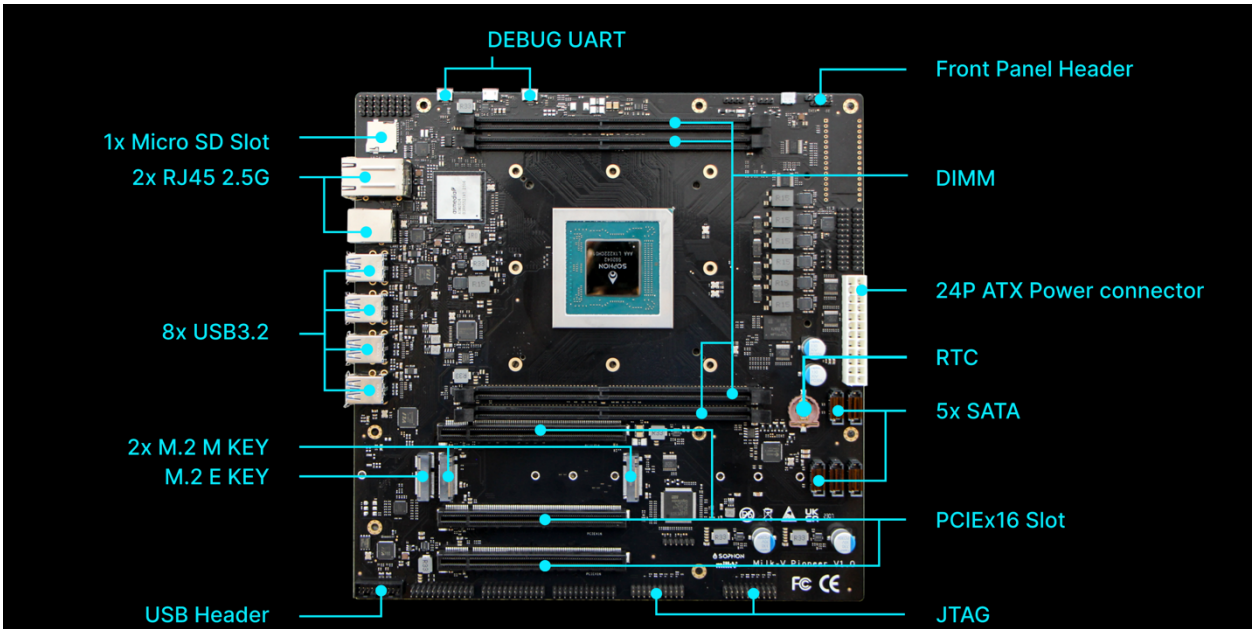
RISC-V for Middle systems

Milk-V Pioneer is a developer motherboard based on SOPHON SG2042 in a standard mATX form factor. With PC-like interfaces and PC industrial compability, Pioneer provides native RISC-V development environment and RISC-V desktop experience. It is the first choice for RISC-V developers and hardware pioneers to experience the cutting-edge technology of RISC-V.



RISC-V for Payment systems

RISC-V architecture can be utilized for payment processing applications, offering several potential advantages.

Cost Efficiency: RISC-V's license-free nature eliminates the need for royalties or licensing costs associated with proprietary architectures. This can result in cost savings for payment processing companies, making RISC-V an attractive option for reducing expenses while maintaining performance and functionality.

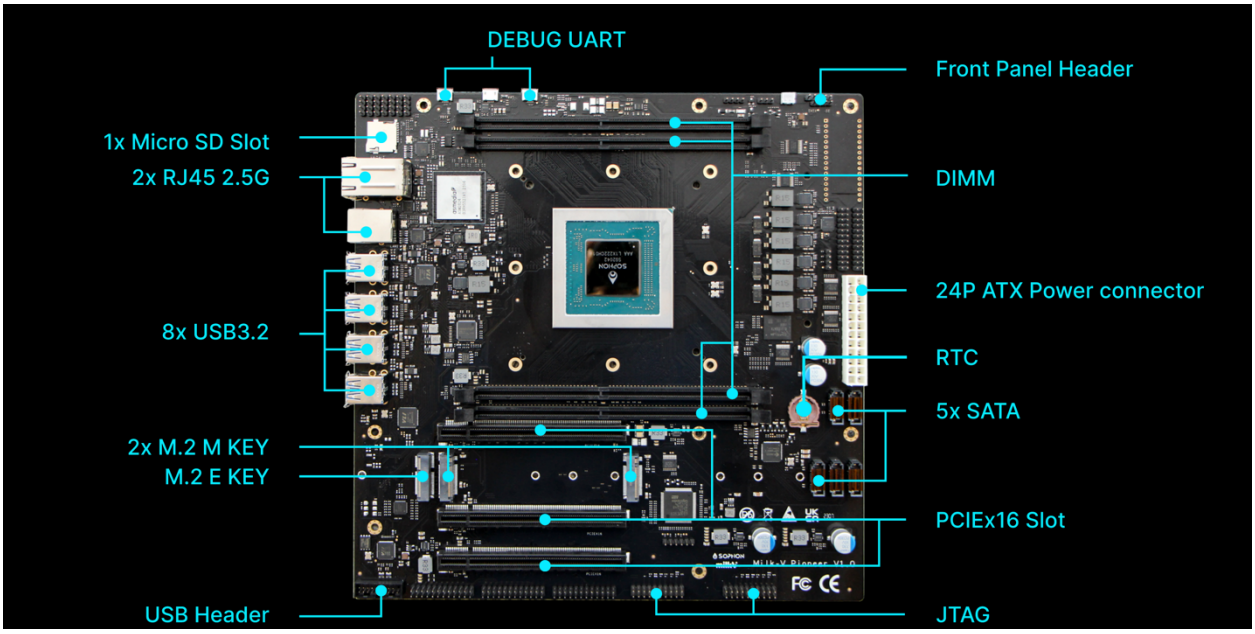
Vendor Independence: RISC-V's license-free nature promotes vendor independence, enabling payment processing companies to choose their hardware suppliers or even develop their own processors internally. This independence reduces the risk of vendor lock-in, provides flexibility in hardware selection, and allows for greater control over the supply chain.

Scalability: RISC-V processors offer scalability, allowing payment processing companies to select the appropriate level of performance and functionality based on their specific needs. Whether it's low-power embedded devices for point-of-sale (POS) terminals or high-performance servers for transaction processing, RISC-V processors can be designed to scale accordingly.

Customization: RISC-V's license-free nature allows payment processing companies to customize the architecture to meet their specific requirements. They can tailor the processor design and instruction set to optimize performance, power efficiency, and security features relevant to payment processing applications. Alibaba Group Holding's chip unit T-Head and Alipay, the payment service under Alibaba's financial affiliate Ant Group, will release computing chips for secure payments based on the RISC-V instruction set architecture, the two entities said. The development comes as Chinese companies continue to invest heavily in chips, in the wake of U.S. export restrictions targeting China's semiconductor sector. The chip will be embedded in hardware devices and used to enhance mobile payments, which are popular in China via the use of QR codes, Alipay and T-Head said on Thursday.

Templado System Payment Gateway

Templado system RISC-V gateway was developed using the following RISC-V hardware:
Pioneer board from Milk-V

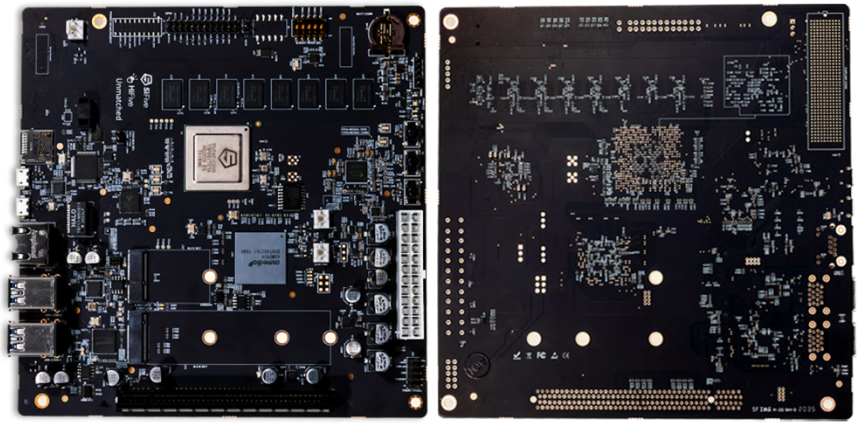


SOPHGO SG2042 Chip
- 64 Core RISC-V CPU up to 2GHz
- 4x DDR4 DIMM slots up to 128GB ram support
- 3x PCIe x16 Slot(PCIe 3.0 x8)
- 5x SATA
- 8x USB3
- 2x M.2 M KEY(PCIe 3.0 x4)
- 1x M.2 E KEY(PCIe 3.0 x1 + USB 2.0)
- 2x RJ45 2.5G
- 1x USB Header for front panel(2x USB 3.0)
- 1x misc header for front panel power, reset, LED etc
- 2x JTAG debug port

- 1x micro USB debug console
- 1x micro SD card for recovery or OS loading
- 1x SPI flash for BIOS

And

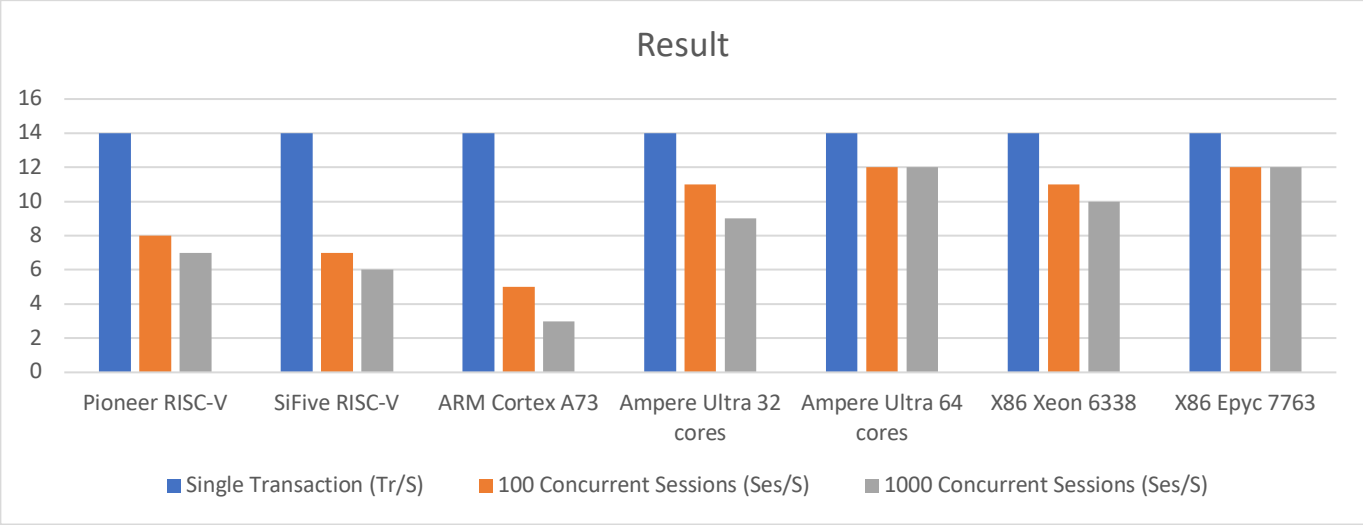
HiFive Unmatched from SiFive



SiFive Freedom U740 (FU740), an SoC that includes a high-performance multi-core, 64-bit dual-issue, superscalar RISC-V processor (SiFive Essential™ U74-MC) with 16GB of DDR4, Gigabit Ethernet, PCIe expansion, USB 3, and M.2 sockets for Wi-Fi, Bluetooth and NVMe storage.

Testing

1. Pioneer Board
2. SiFive Board
3. ARM Cortex A73 CPU, 8GB RAM
4. Ampere Ultra Ampere Altra 32 Core, 32GB RAM, Samsung 970 NVMe, Ubuntu 22.04 Server
5. Ampere Ultra Ampere Altra 64 Core, 32GB RAM, Samsung 970 NVMe, Ubuntu 22.04 Server
6. Dell Power Edge 650. Intel Xeon 6338, 32GB RAM, SATA SSD RAID 5, Microsoft 2019 Server
7. EPYC 7763, 32GB RAM, SATA SSD RAID 5, Microsoft 2019 Server



Transaction Engine was bult using GCC C / C++ plus some Assembly optimization.
For RISC-V binutils + gcc riscv64 was used.

Database was implemented as MariaDB Community Edition.

Single Session / Single transaction takes 64ms to completed on any system. Gateway take around 64ms to process single transaction. All systems perform the same.

Next, we simulate 100 Concurrent Sessions from Apache passing transaction to Transaction Engine
While Ampere 32 core perform on pair with Intel Xeon, but slower than AMD Epyc.
Ampere 64 core slightly outperform Intel Xeon and pretty much the same as AMD Epyc.
Pioneer Board and SiFive outperform ARM Cortex A73, but falling behind of Ampere, Intel and AMD.

Finally, we simulate 1000 Concurrent Sessions from Apache passing transaction to Transaction Engine. This time Pioneer Board and SiFive outperform ARM Cortex A73, but falling significantly behind of Ampere, Intel and AMD.

Conclusion

While ARM has been a dominant architecture in the mobile and embedded markets for many years, RISC-V offers an alternative that allows for more flexibility and customization. However, it's worth noting that ARM has a well-established ecosystem, including a wide range of processors, development tools, and software support, which RISC-V is still catching up with.

In terms of maturity and adoption, ARM has a significant head start over RISC-V. ARM-based processors have been widely used and optimized for various applications, including mobile devices, servers, and embedded systems. On the other hand, RISC-V is still in the process of expanding its ecosystem, and its adoption in commercial products is not as widespread.

The adoption of a RISC-V payment gateway offers several significant benefits:

1. RISC-V has the potential to catch up and offer compelling alternatives in the future, especially considering its open-source nature and growing community support.

2. RISC-V is an open-source instruction set architecture (ISA) that allows for the design and development of custom processors and hardware accelerators. It offers flexibility and customization options, making it an attractive choice for payment gateways.

3. Thanks to its open-source approach, independent from any company or country, RISC-V represents a real alternative to the dominant architectures of Intel x86 and ARM. RISC-V is rapidly emerging to profoundly disrupt the global semiconductor and computing industry.

4. Once Veyron V1 chip and LeapFive NB2 RISC-V will become more widespread and available, it will be a logical step to implement payment gateway to such platform to gain independence.

The idea of implementing a small to medium payment gateway using existing RISC-V solutions is certainly possible. RISC-V is an open-source instruction set architecture (ISA) that provides flexibility and allows for customization, making it a viable option for various applications, including payment systems.

At the moment, RISC-V is more commonly found in embedded systems, microcontrollers, and IoT devices. These applications often require low power consumption, low cost, and customization options, which RISC-V provides. However, as server-class CPUs based on RISC-V enter the market, it could potentially open doors for larger payment systems to adopt the RISC-V platform. Server-class CPUs based on RISC-V would need to meet the performance, scalability, and security requirements of large-scale payment systems.

The RISC-V platform can potentially offer economic benefits and help mitigate concerns related to sanctions. RISC-V is an open-source architecture, which means it does not require expensive licensing fees associated with proprietary architectures. This can lead to cost savings, particularly for companies and organizations looking to develop and deploy their own processors or systems based on the RISC-V platform.

It's important to note that while RISC-V offers potential economic benefits and can help mitigate concerns related to sanctions, other factors beyond the choice of architecture may still impact the overall economic and sanction-free environment. These include regulatory frameworks, geopolitical considerations, and market dynamics.